ACSL-6xx0

Multi-Channel and Bi-Directional, 15 MBd Digital Logic Gate Optocoupler

Data Sheet



Lead (Pb) Free
RoHS 6 fully compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

ACSL-6xx0 are truly isolated, multi-channel and bi-directional, high-speed optocouplers. Integration of multiple optocouplers in monolithic form is achieved through patented process technology. These devices provide full duplex and bi-directional isolated data transfer and communication capability in compact surface mount packages. Available in 15 Mbd speed option and wide supply voltage range.

These high channel density make them ideally suited to isolating data conversion devices, parallel buses and peripheral interfaces.

They are available in 8-pin and 16–pin narrow-body SOIC package and are specified over the temperature range of -40°C to +100°C.

Features

- Available in dual, triple and quad channel configurations
- Bi-directional
- Wide supply voltage range: 3.0V to 5.5V
- High-speed: 15 MBd typical, 10 MBd minimum
- 10 kV/µs minimum Common Mode Rejection (CMR) at Vcm = 1000V
- LSTTL/TTL compatible
- Safety and regulatory approvals
  - 2500Vrms for 1 min per UL1577
  - cUL (CSA Component Acceptance Notice 5A)
  - IEC/EN/DIN EN 60747-5-5
- 16 Pin narrow-body SOIC package for triple and quad channel
- -40 to 100°C temperature range

Applications

- Serial Peripheral Interface (SPI)
- Inter-Integrated Interface (I2C)
- Full duplex communication
- Isolated line receiver
- Microprocessor system interfaces
- Digital isolation for A/D and D/A conversion
- Instrument input/output isolation
- Ground loop elimination

CAUTION: *It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD. The components featured in this datasheet are not to be used in military or aerospace applications or environments.*

Device Selection Guide

Device Number	Channel Configuration	Package
ACSL-6210	Dual, Bi-Directional`	8-pin Small Outline
ACSL-6300	Triple, All-in-One	16-pin Small Outline
ACSL-6310	Triple, Bi-Directional, 2/1	16-pin Small Outline
ACSL-6400	Quad, All-in-One	16-pin Small Outline
ACSL-6410	Quad, Bi-Directional, 3/1	16-pin Small Outline
ACSL-6420	Quad, Bi-Directional, 2/2	16-pin Small Outline

Ordering Information

ACSL-6xx0 is UL Recognized with 2500 V_{rms} for 1 minute per UL1577 and is approved under CSA Component Acceptance Notice #5, File CA 88324.

Part number	RoHS Compliant[1]	Package	Surface Mount	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity
ACSL-6210	-00RE	SO-8	X			100 per tube
	-06RE	SO-8	X		X	100 per tube
	-50RE	SO-8	X	X		1500 per reel
	-56RE	SO-8	X	X	X	1500 per reel
ACSL-6300 ACSL-6310 ACSL-6400 ACSL-6410 ACSL-6420	-00TE	SO-16	X			50 per tube
	-06TE	SO-16	X		X	50 per tube
	-50TE	SO-16	X	X		1000 per reel
	-56TE	SO-16	X	X	X	1000 per reel

Note 1: The ACSL-6xx0 product family is only offered in RoHS compliant option.

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACSL-6210-56RE refers to ordering a Surface Mount SO-8 package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Example 2:

ACSL-6400-00TE refers to ordering a Surface Mount SO-16 package product in tube packaging and in RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Pin Description

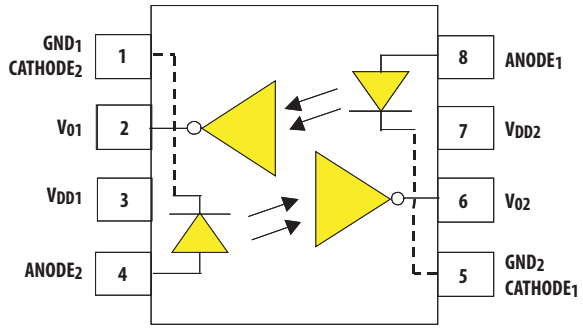
Symbol	Description	Symbol	Description
V_{DD1}	Power Supply 1	GND_1	Power Supply Ground 1
V_{DD2}	Power Supply 2	GND_2	Power Supply Ground 2
$ANODE_x$	LED Anode	NC	Not Connected
$CATHODE_x$	LED Cathode	V_{OX}	Output Signal

Truth Table (Positive Logic)

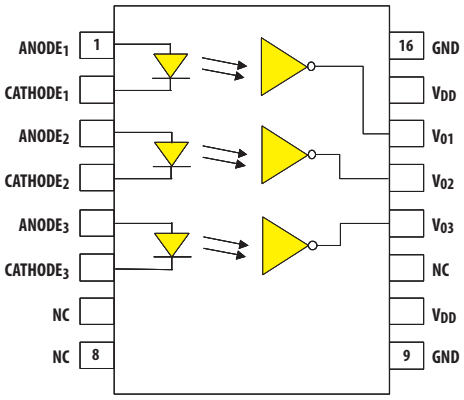
LED	OUTPUT
ON	L
OFF	H

Functional Diagrams

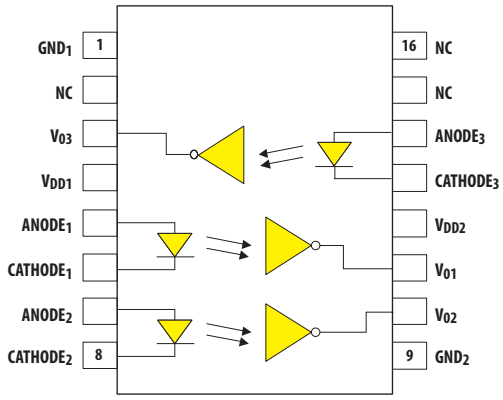
ACSL-6210 - Dual-Ch, Bi-Dir



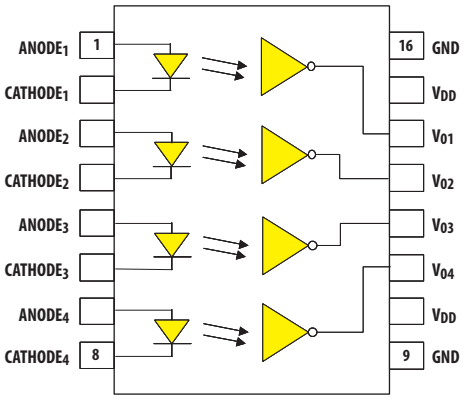
ACSL-6300 - Triple-Ch, All-in-One



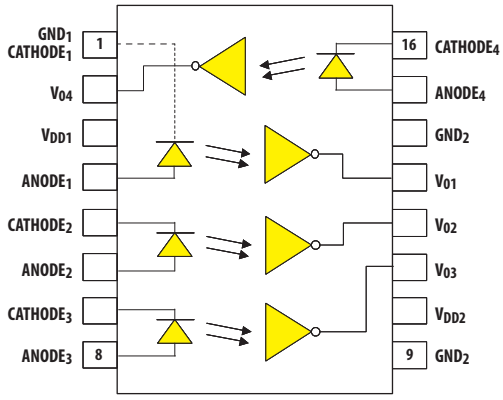
ACSL-6310 - Triple-Ch, Bi-Dir (2/1)



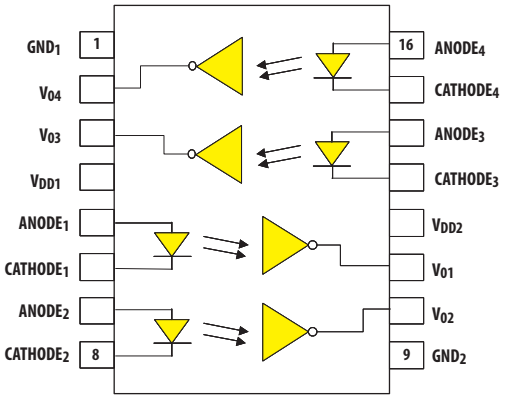
ACSL-6400 - Quad-Ch, All-in-One



ACSL-6410 - Quad-Ch, Bi-Dir (3/1)



ACSL-6420 - Quad-Ch, Bi-Dir (2/2)



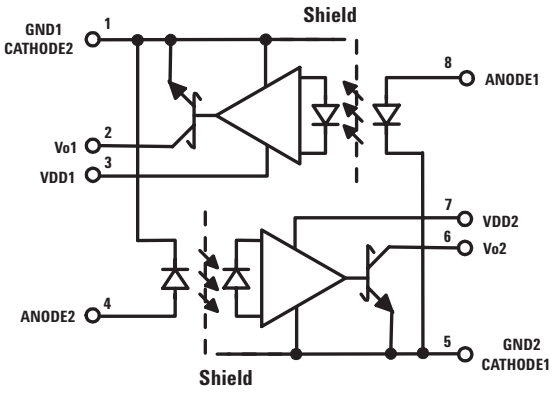
Schematic Diagrams

The ACSL-6xx0 series optocouplers feature the GaAsP LEDs with proprietary back emission design. They offer the designer a broad range of input drive current, from 7 mA to 15 mA, thus providing greater flexibility in designing the drive circuit.

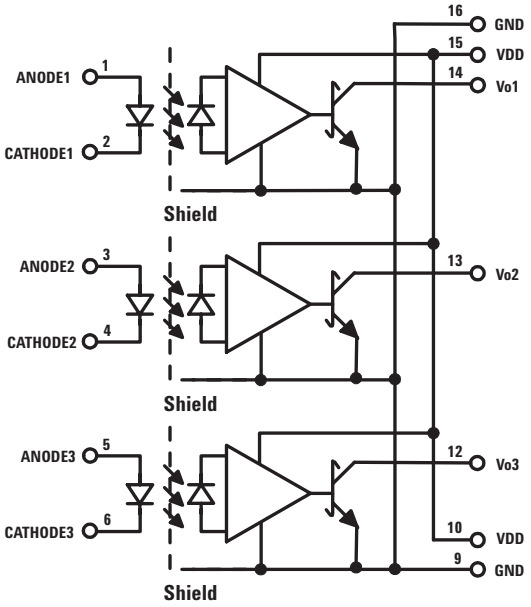
The output detector integrated circuit (IC) in the optocoupler consists of a photodiode at the input of a two-stage amplifier that provides both high gain and high bandwidth. The secondary amplifier stage of the detector IC feeds into an open collector Schottky-clamped transistor.

The entire output circuit is electrically shielded so that any common-mode transient capacitively coupled from the LED side of the optocoupler is diverted from the photodiode to ground. With this electric shield, the optocoupler can withstand transients that slopes up to 10,000V/µs, and amplitudes up to 1,000V.

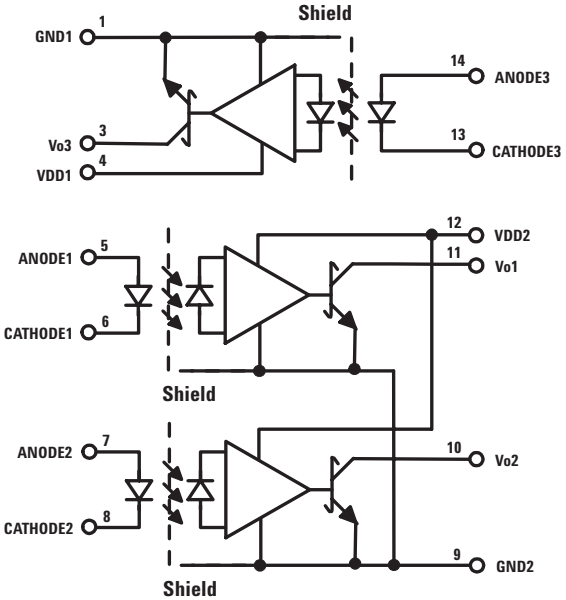
ACSL-6210 - Dual-Ch, Bi-Dir



ACSL-6300 - Triple-Ch, All-in-One

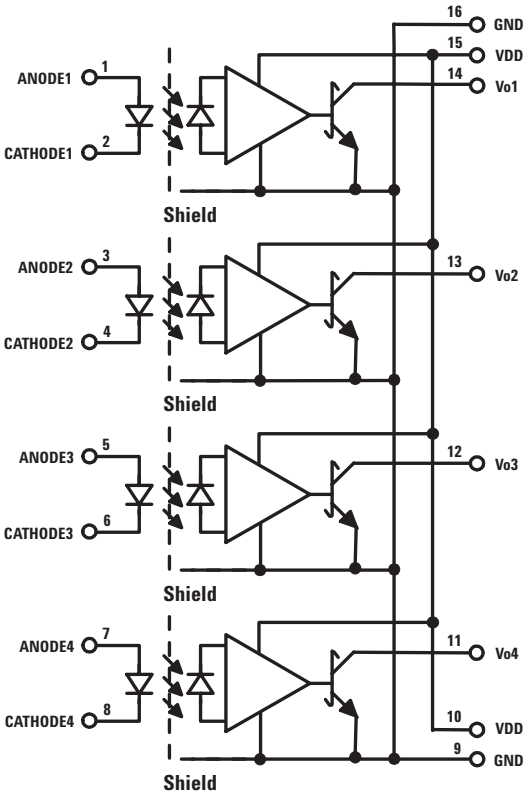


ACSL-6310 - Triple-Ch, Bi-Dir (2/1)

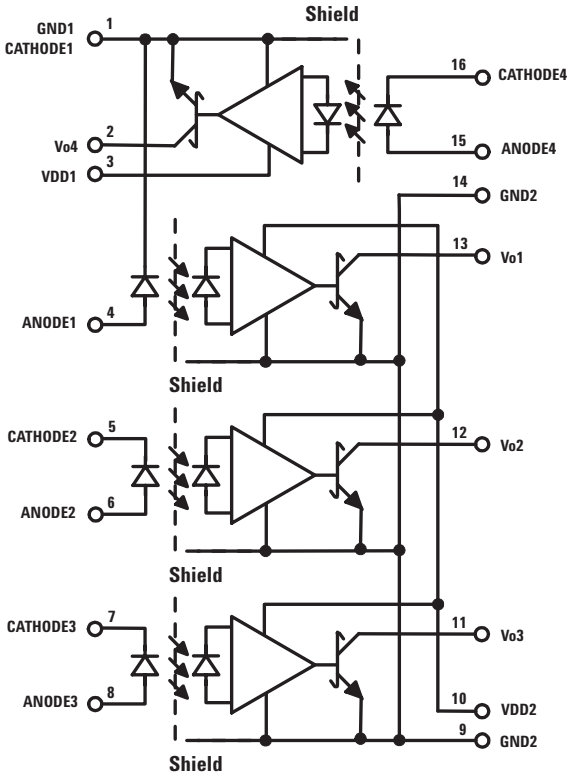


Schematic Diagrams, continued

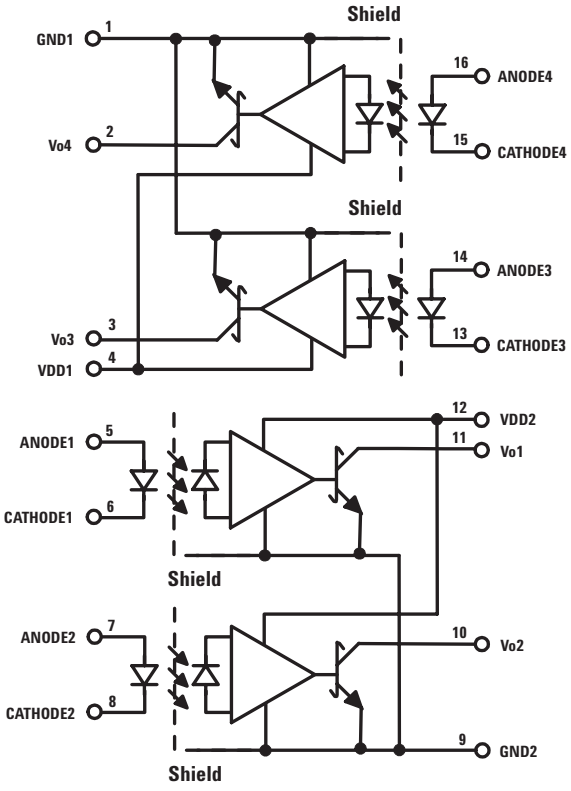
ACSL-6400 - Quad-Ch, All-in-One



ACSL-6410 - Quad-Ch, Bi-Dir (3/1)

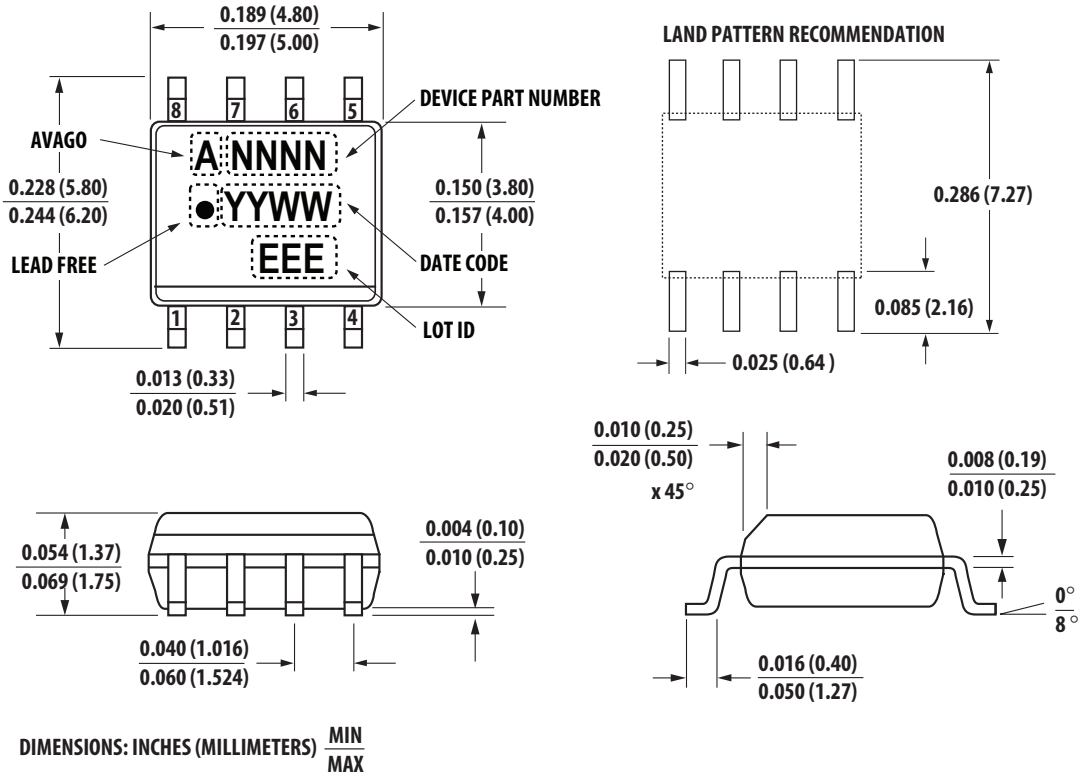


ACSL-6420 - Quad-Ch, Bi-Dir (2/2)



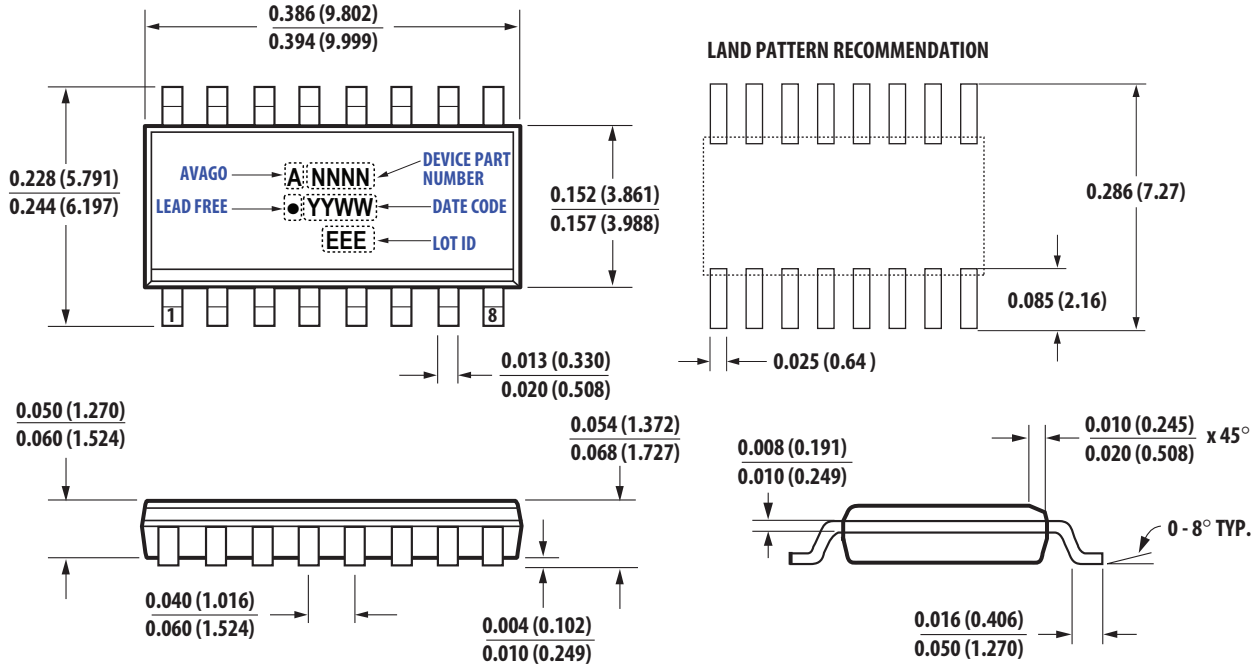
Package Outline Drawings

ACSL-6210 Small Outline SO-8 Package



DIMENSIONS: INCHES (MILLIMETERS) MIN / MAX

ACSL-6300, ACSL-6310, ACSL-6400, ACSL-6410 and ACSL-6420 Small Outline SO-16 Package



DIMENSIONS: INCHES (MILLIMETERS) MIN / MAX

Reflow Soldering Profile

The recommended reflow soldering conditions are per JEDEC Standard J-STD-020 (latest revision). Non-halide flux should be used.

Regulatory Information

Insulation and Safety Related Specifications

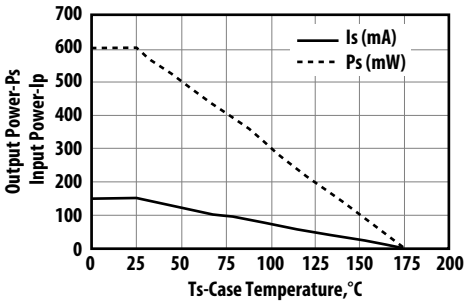
Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L(I01)	4.9	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum Externa l Tracking (Creepage)	L(I02)	4.5	mm	Measured from input terminals to output terminals, shortest distance path through body
Minimum Internal Plastic Gap (Internal Clearance)		0.08	mm	Insulation thickness between emitter and detector; also known as distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	175	Volts	DIN IEC 112/VDE0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

IEC/EN/DIN EN 60747-5-5 Insulation Characteristics* (Option x6xx)

Description	Symbol	Characteristic	Unit
Installation classification per DIN VDE 0110, Table 1 for rated mains voltage ≤ 150 Vrms for rated mains voltage ≤ 300 Vrms		 I – IV I – III	
Climatic Classification		40/100/21	
Pollution Degree (DIN VDE 0110/39)		2	
Maximum Working Insulation Voltage	V_{IORM}	567	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m=1 sec, Partial discharge < 5 pC	V_{PR}	1063	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.6 = V_{PR}, Type and Sample Test, t_m=10 sec, Partial discharge < 5 pC	V_{PR}	907	V_{peak}
Highest Allowable Overvoltage (Transient Overvoltage t_{ini} = 60 sec)	V_{IOTM}	4000	V_{peak}
Safety-limiting values – maximum values allowed in the event of a failure. Case Temperature Input Current** Output Power**	 T_S $I_{S, INPUT}$ $P_{S, OUTPUT}$	 175 150 600	 °C mA mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$>10^9$	Ω

* Refer to the optocoupler section of the Isolation and Control Components Designer's Catalog, under Product Safety Regulations section, (IEC/EN/DIN EN 60747-5-5) for a detailed description of Method a and Method b partial discharge test profiles.

** Refer to following figure for dependence of PS and IS on ambient temperature.



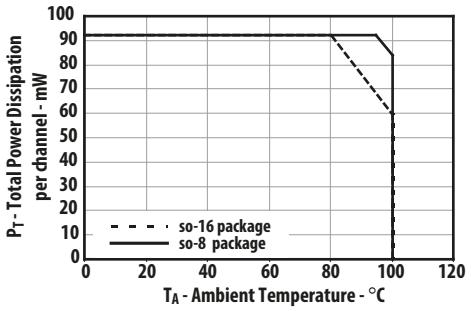
Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	T_s	-55	125	°C
Operating Temperature	T_A	-40	100	°C
Supply Voltage (1 Minute Maximum)	V_{DD1} , V_{DD2}		7	V
Reverse Input Voltage (Per Channel)	V_R		5	V
Output Voltage (Per Channel)	V_O		7	V
Average Forward Input Current[1] (Per Channel)	I_F		15	mA
Output Current (Per Channel)	I_O		50	mA
Input Power Dissipation[2] (Per Channel)	P_I		27	mW
Output Power Dissipation[2] (Per Channel)	P_O		65	mW

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Operating Temperature	T_A	-40	100	°C
Input Current, Low Level[3]	I_{FL}	0	250	µA
Input Current, High Level[4]	I_{FH}	7	15	mA
Supply Voltage	V_{DD1}, V_{DD2}	3.0	5.5	V
Fan Out (at R_L = 1kΩ)	N		5	TTL Loads
Output Pull-up Resistor	R_L	330	4k	Ω

Notes:
1. Peaking circuits may produce transient input currents up to 50 mA, 50 ns max. pulse width, provided average current does not exceed its max. values.
2. Derate total package power dissipation, PT linearly above +95°C free-air temperature at a rate of 1.57mW/°C for the SO8 package mounted on low conductivity board per JESD 51-3. Derate total package power dissipation, PT linearly above +80°C free-air temperature at a rate of 1.59 mW/°C for the SO16 package mounted on low conductivity board per JESD 51-3. PT= number of channels multiplied by (PI+PO).
3. The off condition can be guaranteed by ensuring that $V_{FL} \leq 0.8V$.
4. The initial switching threshold is 7 mA or less. It is recommended that minimum 8 mA be used for best performance and to permit guardband for LED degradation.



Electrical Specifications

Over recommended operating range (3.0V ≤ V_{DD1} ≤ 3.6V, 3.0V ≤ V_{DD2} ≤ 3.6V, T_A = -40°C to +100°C) unless otherwise specified. All typical specifications are at T_A = +25°C , V_{DD1} = V_{DD2} = +3.3V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Threshold Current	I_{TH}		2.7	7.0	mA	$I_{OL(Sinking)}$=13 mA, V_O= 0.6V
High Level Output Current	I_{OH}		4.7	100.0	µA	I_F = 250 µA, V_O = 3.3V
Low Level Output Voltage	V_{OL}		0.36	0.68	V	$I_{OL(Sinking)}$ = 13 mA, I_F = 7mA
High Level Supply Current (per channel)	I_{DDH}		3.2	5.0	mA	I_F = 0 mA
Low Level Supply Current (per channel)	I_{DDL}		4.6	7.5	mA	I_F = 10 mA
Input Forward Voltage	V_F	1.25	1.52	1.80	V	I_F = 10 mA, T_A = 25°C
Input Reverse Breakdown Voltage	BV_R	5.0			V	I_R = 10 µA
Input Diode Temperature Coefficient	$\Delta V_F / \Delta T_A$		-1.8		mV/°C	I_F = 10 mA
Input Capacitance	C_{IN}		80		pF	f = 1 MHz, V_F = 0V

Switching Specifications

Over recommended operating range (3.0V ≤ V_{DD1} ≤ 3.6V, 3.0V ≤ V_{DD2} ≤ 3.6V, I_F = 8.0 mA, T_A = -40°C to +100°C) unless otherwise specified. All typical specifications are at T_A = +25°C , V_{DD1} = V_{DD2} = +3.3V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Maximum Data Rate		10	15		MBd	R_L = 350Ω, C_L = 15 pF
Pulse Width	t_{PW}	100			ns	R_L = 350Ω, C_L = 15 pF
Propagation Delay Time to Logic High Output Level [5]	t_{PLH}		52	100	ns	R_L = 350Ω, C_L = 15 pF
Propagation Delay Time to Logic Low Output Level [6]	t_{PHL}		44	100	ns	R_L = 350Ω, C_L = 15 pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	|PWD|		8	35	ns	R_L = 350Ω, C_L = 15 pF
Propagation Delay Skew [7]	t_{PSK}			40	ns	R_L = 350Ω, C_L = 15 pF
Output Rise Time (10 – 90%)	t_R		35		ns	R_L = 350Ω, C_L = 15 pF
Output Fall Time (10 – 90%)	t_F		12		ns	R_L = 350Ω, C_L = 15 pF
Logic High Common Mode Transient Immunity [8]	|CM_H|	10			kV/µs	V_{cm} = 1000V, I_F = 0 mA, V_O = 2.0V, R_L = 350Ω, T_A = 25°C
Logic Low Common Mode Transient Immunity [8]	|CM_L|	10			kV/µs	V_{cm} = 1000V, I_F = 8 mA, V_O = 0.8V, R_L = 350Ω, T_A = 25°C

Notes:

5. t_{PLH} is measured from the 4.0 mA level on the falling edge of the input pulse to the 1.5V level on the rising edge of the output pulse.
6. t_{PHL} is measured from the 4.0 mA level on the rising edge of the input pulse to the 1.5V level on the falling edge of the output pulse.
7. t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature and specified test conditions.
8. CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining V_O > 2.0V. CM_L is the maximum common mode voltage slew rate that can be sustained while maintaining V_O < 0.8V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.

Electrical Specifications

Over recommended operating range (4.5V ≤ V_{DD1} ≤ 5.5V, 4.5V ≤ V_{DD2} ≤ 5.5V, T_A = -40°C to +100°C) unless otherwise specified. All typical specifications are at T_A = +25°C, V_{DD1} = V_{DD2} = +5.0V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input Threshold Current	I_{TH}		2.7	7.0	mA	$I_{OL(Sinking)}$=13 mA, V_O= 0.6V
High Level Output Current	I_{OH}		3.8	100.0	µA	I_F = 250 µA, V_O= 5.5V
Low Level Output Voltage	V_{OL}		0.36	0.6	V	$I_{OL(Sinking)}$=13 mA, I_F=7 mA
High Level Supply Current (per channel)	I_{DDH}		4.3	7.5	mA	I_F = 0 mA
Low Level Supply Current (per channel)	I_{DDL}		5.8	10.5	mA	I_F = 10 mA
Input Forward Voltage	V_F	1.25	1.52	1.8	V	I_F = 10 mA, T_A = 25°C
Input Reverse Breakdown Voltage	BV_R	5.0			V	I_R = 10 µA
Input Diode Temperature Coefficient	$\Delta V_F / \Delta T_A$		-1.8		mV/°C	I_F = 10 mA
Input Capacitance	C_{IN}		80		pF	f = 1 MHz, V_F = 0V

Switching Specifications

Over recommended operating range (4.5V ≤ V_{DD1} ≤ 5.5V, 4.5V ≤ V_{DD2} ≤ 5.5V, I_F = 8.0 mA, T_A = -40°C to +100°C) unless otherwise specified. All typical specifications are at T_A=+25°C, V_{DD1} = V_{DD2} = +5.0V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Maximum Data Rate		10	15		MBd	R_L = 350Ω, C_L =15 pF
Pulse Width	t_{PW}	100			ns	R_L = 350Ω, C_L =15 pF
Propagation Delay Time to Logic High Output Level[5]	t_{PLH}		46	100	ns	R_L = 350Ω, C_L =15 pF
Propagation Delay Time to Logic Low Output Level[6]	t_{PHL}		43	100	ns	R_L = 350Ω, C_L =15 pF
Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	|PWD|		5	35	ns	R_L = 350Ω, C_L =15 pF
Propagation Delay Skew[7]	t_{PSK}			40	ns	R_L = 350Ω, C_L =15 pF
Output Rise Time (10 – 90%)	t_R		30		ns	R_L = 350Ω, C_L =15 pF
Output Fall Time (10 – 90%)	t_F		12		ns	R_L = 350Ω, C_L =15 pF
Logic High Common Mode Transient Immunity [8]	|CM_H|	10			kV/µs	V_{cm}= 1000V, I_F=0 mA, V_O= 2.0V, R_L=350Ω, T_A= 25°C
Logic Low Common Mode Transient Immunity [8]	|CM_L|	10			kV/µs	V_{cm}= 1000V, I_F= 8 mA, V_O= 0.8V, R_L= 350Ω, T_A= 25°C

Notes:

5. t_{PLH} is measured from the 4.0 mA level on the falling edge of the input pulse to the 1.5V level on the rising edge of the output pulse.
6. t_{PHL} is measured from the 4.0 mA level on the rising edge of the input pulse to the 1.5V level on the falling edge of the output pulse.
7. t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature and specified test conditions.
8. CM_H is the maximum common mode voltage slew rate that can be sustained while maintaining V_O > 2.0V. CM_L is the maximum common mode voltage slew rate that can be sustained while maintaining V_O < 0.8V. The common mode voltage slew rates apply to both rising and falling common mode voltage edges.

Package Characteristics

All specifications are at T_A=+25°C.

Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Input-Output Momentary Withstand Voltage[9]	SO8 SO16	V_{ISO} V_{ISO}	2500 2500			V_{RMS}	RH ≤ 50%, t = 1 min RH≤50%, t = 1 min
Input-Output Insulation[10] [11]	SO8 SO16	I_{I-O} I_{I-O}			5 5	µA	45% RH, t=5 sec, V_{I-O}= 3kV DC 45% RH, t = 5 sec, V_{I-O}=3kV DC
Input-Output Resistance[10]	SO8 SO16	R_{I-O} R_{I-O}	10^9 10^9	10^{11} 10^{11}		Ω	V_{I-O}= 500V DC V_{I-O}= 500V DC
Input-Output Capacitance[10]	SO8 SO16	C_{I-O} C_{I-O}		0.7 0.7		pF	f = 1 MHz f = 1 MHz
Input-Input Insulation Leakage Current[12]	SO8 SO16	I_{I-I} I_{I-I}		0.005 0.005		µA	RH ≤ 45%, t=5 sec, V_{I-I}=500V RH≤45%, t=5 sec, V_{I-I}=500V
Input-Input Resistance[12]	SO8 SO16	R_{I-I} R_{I-I}		10^{11} 10^{11}		Ω	RH≤45%, t = 5 sec, V_{I-I}=500V RH≤45%, t=5 sec, V_{I-I}=500V
Input-Input Capacitance[12]	SO8 SO16	C_{I-I} C_{I-I}		0.1 0.12		pF	f = 1 MHz f = 1 MHz

Notes:

9. V_{ISO} is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For continuous voltage rating, refer to the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table (if applicable), the equipment level safety specification or Avago Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."
10. Measured between each input pair shorted together and all output connections for that channel shorted together.
11. In accordance to UL1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 Vrms for 1 sec (leakage detection current limit, I_{I-O} ≤ 5 µA). This test is performed before the 100% production test for partial discharge (Method b) shown in the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table, if applicable.
12. Measured between inputs with the LED anode and cathode shorted together.

Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, Avago recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Typical Performance

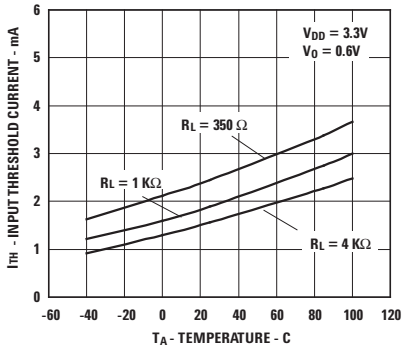


Figure 1. Typical input threshold current vs. temperature for 3.3V operation.

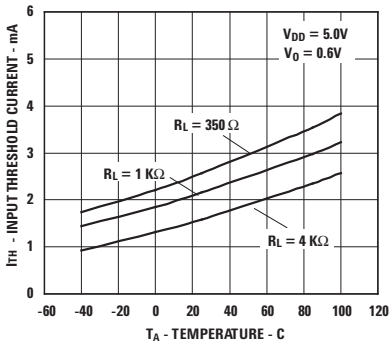


Figure 2. Typical input threshold current vs. temperature for 5V operation.

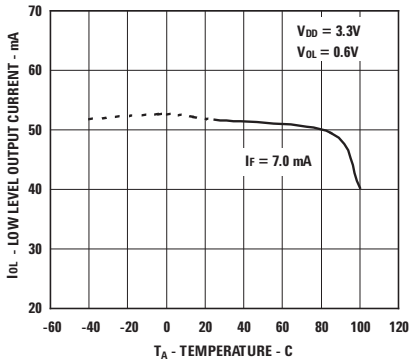


Figure 3. Typical low level output current vs. temperature for 3.3V operation.

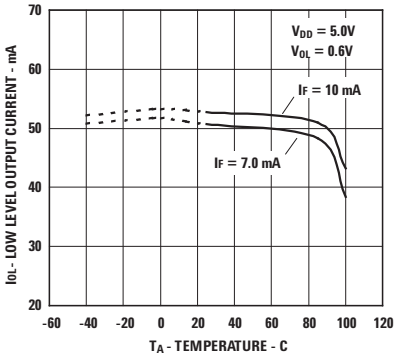


Figure 4. Typical low level output current vs. temperature for 5V operation.

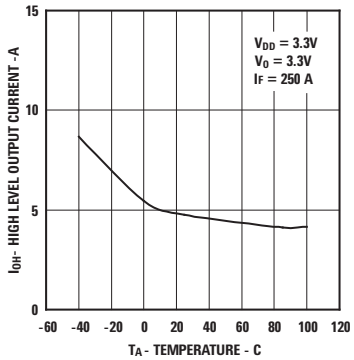


Figure 5. Typical high level output current vs. temperature for 3.3V operation.

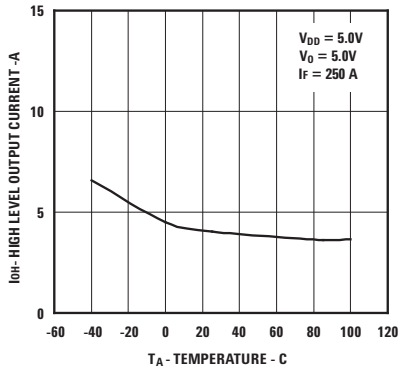


Figure 6. Typical high level output current vs. temperature for 5V operation.

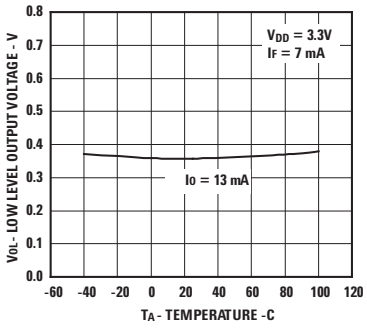


Figure 7. Typical low level output voltage vs. temperature for 3.3V operation.

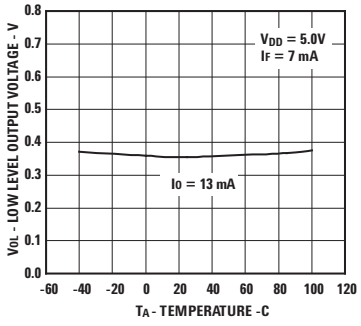


Figure 8. Typical low level output voltage vs. temperature for 5V operation.

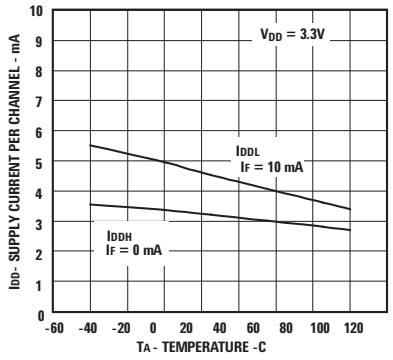


Figure 9. Typical supply current per channel vs. temperature for 3.3V operation.

Typical Performance, continued

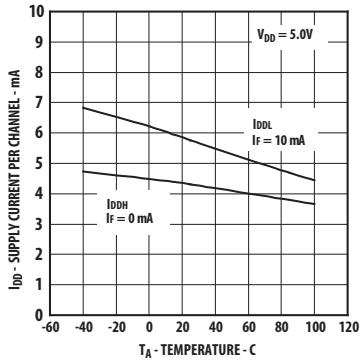


Figure 10. Typical supply current per channel vs. temperature for 5V operation.

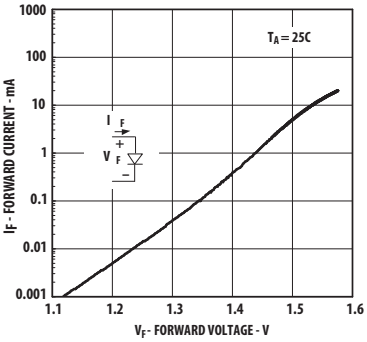


Figure 11. Typical input diode forward characteristics.

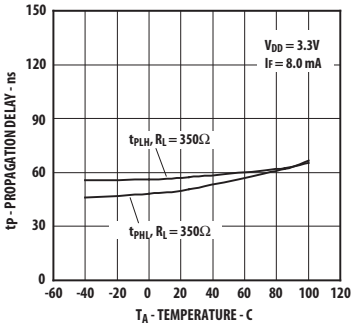


Figure 12. Typical propagation delay vs. temperature for 3.3V operation.

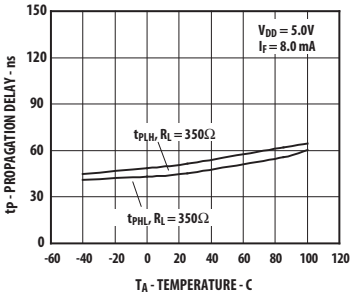


Figure 13. Typical propagation delay vs. temperature for 5V operation.

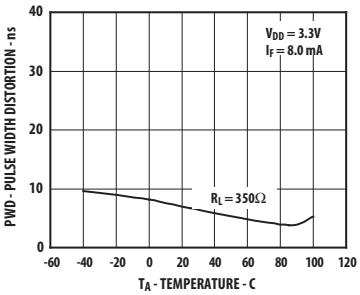


Figure 14. Typical pulse width distortion vs. temperature for 3.3V operation.

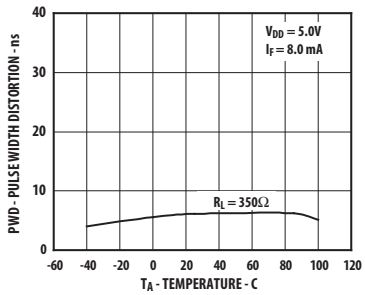
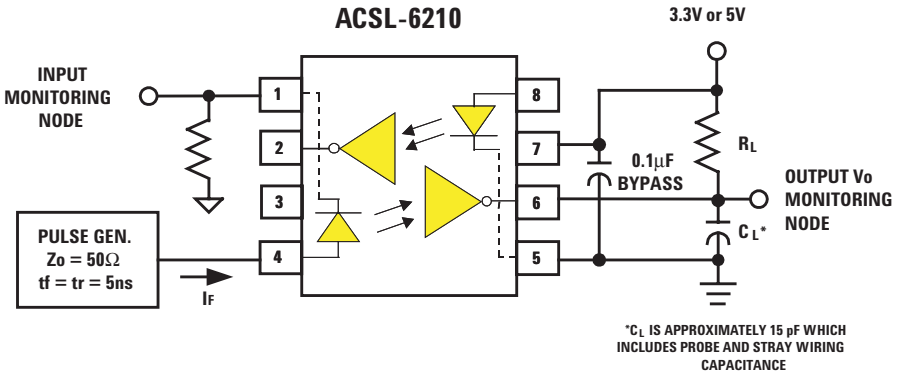


Figure 15. Typical pulse width distortion vs. temperature for 5V operation.

Test Circuits



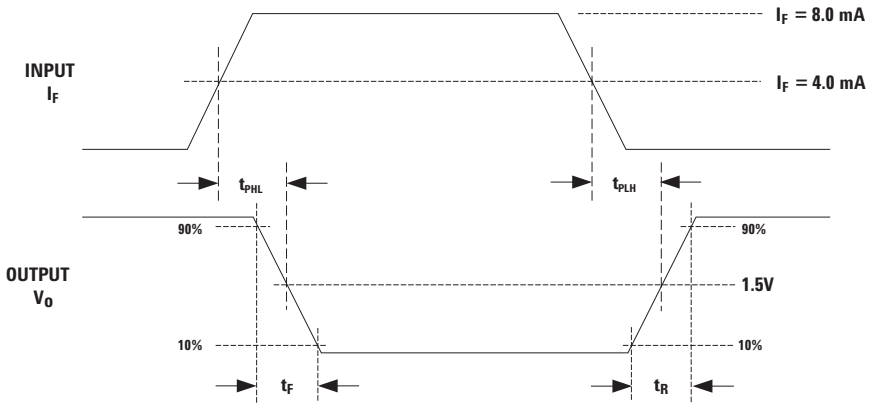


Figure 16. Test circuit for t_{PHL}, t_{PLH}, $t_{r,}$ and t_{R}.

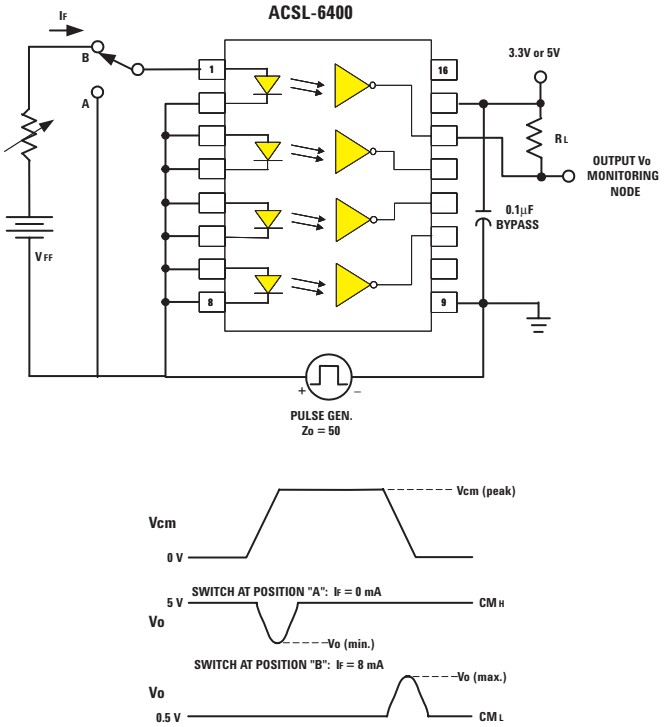


Figure 17. Test circuit for common mode transient immunity and typical waveforms

Figure 17. Test circuit for common mode transient immunity and typical waveforms.

Application Information

ON and OFF Conditions

The ACSL-6xx0 series has the ON condition defined by current, and the OFF condition defined by voltage. In order to guarantee that the optocoupler is OFF, the forward voltage across the LED must be less than or equal to 0.8 volt for the entire operating temperature range. This has direct implications for the input drive circuit. If the design uses a TTL gate to drive the input LED, then one has to ensure that the gate output voltage is sufficient to cause the forward voltage to be less than 0.8 volt. The typical threshold current for the ACSL-6xx0 series optocouplers is 2.7 mA; however, this threshold could increase over time due to the aging effects of the LED. Drive circuit arrangements must provide for the ON state LED forward current of at least 7 mA, or more if faster operation is desired.

Maximum Input Current and Reverse Voltage

The average forward input current should not exceed the 15 mA Absolute Maximum Rating as stated; however, peaking circuits with transient input currents up to 50 mA are allowed provided the average current does not exceed 15 mA. If the input current maximum rating is exceeded, the local temperature of the LED can rise, which in turn may affect the long-term reliability of the device. When designing the input circuit, one must also ensure that the input reverse voltage does not exceed 5 V. If the optocoupler is subjected to reverse voltage transients or accidental situations that may cause a reverse voltage to be applied, thus an anti-parallel diode across the LED is recommended.

Suggested Input Circuits for Driving the LED

Figures 18, 19, and 20 show some of the several techniques for driving the ACSL-6xx0 LED. Figure 18 shows the recommended circuit when using any type of TTL gate. The buffer PNP transistor allows the circuit to be used with TTL or CMOS gates that have low sinking current capability. One advantage of this circuit is that there is very little variation in power supply current due to the switching of the optocoupler LED. This can be important in high-resolution analog-to-digital (A/D) systems where ground loop currents due to the switching of the LEDs can cause distortion in the A/D output.

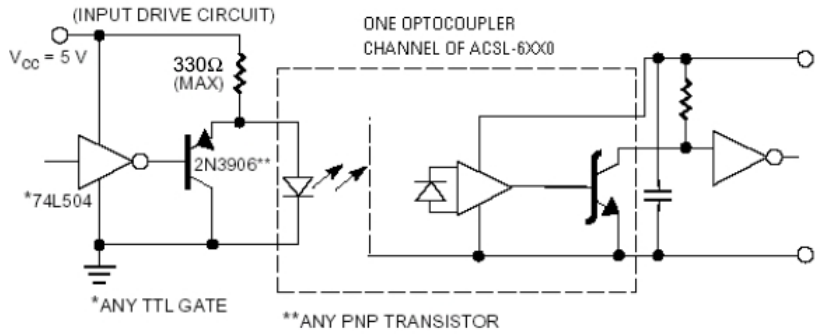


Figure 18. TTL interface circuit for the ACSL-6xx0.

With a CMOS gate to drive the optocoupler, the circuit shown in Figure 19 can be used. The diode in parallel to the current limiting resistor speeds the turn-off of the optocoupler LED. Any HC or HCT series CMOS gate can be used in this circuit.

For high common-mode rejection applications, the drive circuit shown in Figure 20 is recommended. In this circuit, only an open-collector TTL, or an open drain CMOS gate can be used. This circuit drives the optocoupler LED with a 220 ohm current-limiting resistor to ensure that an I_F of 7 mA is applied under worst case conditions and thus guarantee the 10,000 V/µs optocoupler common mode rejection rating. The designer can obtain even higher common-mode rejection performance than 10,000 V/µs by driving the LED harder than 7 mA.

Phase Relationship to Input

The output of the optocoupler is inverted when compared to the input. The input is defined to be logic HIGH when the LED is ON. If there is a design that requires the optocoupler to behave as a non-inverting gate, then the series input drive circuit shown in Figure 19 can be used. This input drive circuit has an inverting function, and since the optocoupler also behaves as an inverter, the total circuit is non-inverting. The shunt drive circuits shown in Figures 18 and 20 will cause the optocoupler to function as an inverter.

Current and Voltage Limitations

The absolute maximum voltage allowable at the output supply voltage pin and the output voltage pin of the optocoupler is 7 volts. However, the recommended maximum voltage at these two pins is 5.5 volts. The output sinking current should not exceed 13 mA in order to make the Low Level Output Voltage be less than 0.6 volt. If the output voltage is not a consideration, then the absolute maximum current allowed through the ACSL-6xx0 is 50 mA. If the output requires switching either higher currents or voltages, output buffer stages as shown in Figures 21 and 22 are suggested.

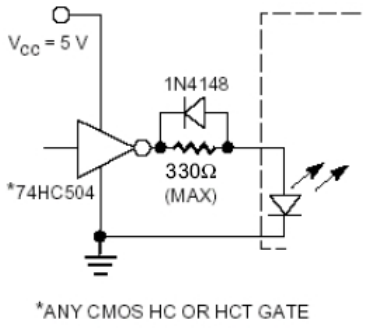


Figure 19. CMOS drive circuit for the ACSL-6xx0.

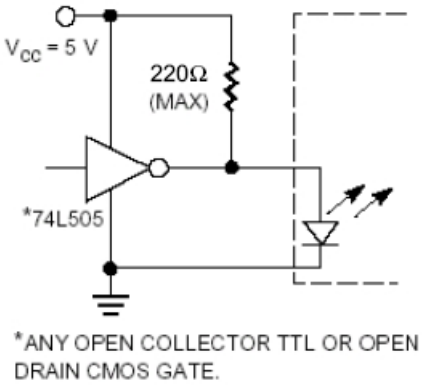


Figure 20. High CMR drive circuit for the ACSL-6xx0.

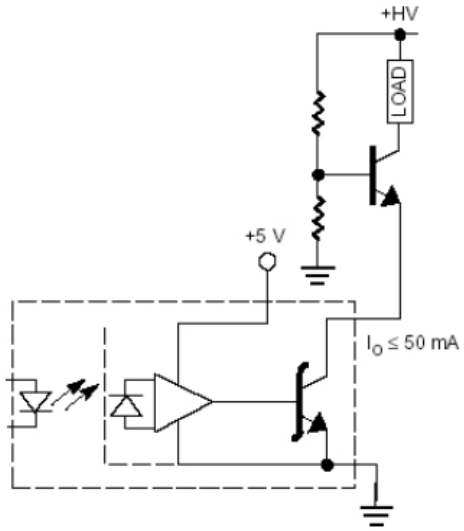


Figure 21. High voltage switching with ACSL-6xx0.

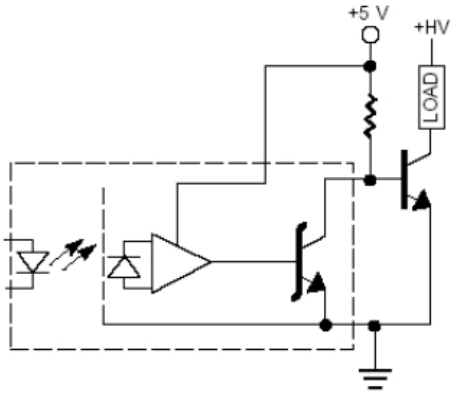


Figure 22. High voltage and high current switching with ACSL-6xx0.

Propagation Delay, Pulse-Width Distortion and Propagation Delay Skew

Propagation delay is a figure of merit which describes how quickly a logic signal propagates through a system. The propagation delay from low to high (t_{PLH}) is the amount of time required for an input signal to propagate to the output, causing the output to change from low to high. Similarly, the propagation delay from high to low (t_{PHL}) is the amount of time required for the input signal to propagate to the output causing the output to change from high to low (see Figure 16).

Pulse-width distortion (PWD) results when t_{PLH} and t_{PHL} differ in value. PWD is defined as the difference between t_{PLH} and t_{PHL} and often determines the maximum data rate capability of a transmission system. PWD can be expressed in percent by dividing the PWD (in ns) by the minimum pulse width (in ns) being transmitted. Typically, PWD on the order of 20-30% of the minimum pulse width is tolerable; the exact figure depends on the particular application (RS232, RS422, T-l, etc.).

Propagation delay skew,t_{PSK}, is an important parameter to consider in parallel data applica- tions where synchronization of signals on parallel data lines is a concern. If the parallel data is being sent through a group of optocouplers, differences in propagation delays will cause the data to arrive at the outputs of the optocouplers at different times. If this difference in propagation delays is large enough, it will determine the maximum rate at which parallel data can be sent through the optocouplers.

Propagation delay skew is defined as the difference between the minimum and maximum propagation delays,either t_{PLH} or t_{PHL}, for any given group of optocouplers which are operating under the same conditions (i.e., the same drive current, supply voltage, output load, and operating temperature). As illustrated in Figure 23, if the inputs of a group of optocouplers are switched either ON or OFF at the same time, t_{PSK} is the difference between the shortest propagation delay,either t_{PLH} or tPHL, and the longest propagation delay,either t_{PLH} or t_{PHL}.

As mentioned earlier,t_{PSK} can determine the maximum parallel data transmission rate. Figure 24 is the timing diagram of a typical parallel data application with both the clock and the data lines being sent through optocouplers. The figure shows data and clock signals at the inputs and outputs of the optocouplers. To obtain the maximum data transmission rate, both edges of the clock signal are being used to clock the data;if only one edge were used, the clock signal would need to be twice as fast.

Propagation delay skew repre- sents the uncertainty of where an edge might be after being sent through an optocoupler. Figure 24 shows that there will be uncertainty in both the data and the clock lines. It is important that these two areas of uncertainty not overlap, otherwise the clock signal might arrive before all of the data outputs have settled,or some of the data outputs may start to change before the clock signal has arrived. From these considerations, the absolute minimum pulse width that can be sent through optocouplers in a parallel application is twice t_{PSK}. A cautious design should use a slightly longer pulse width to ensure that any additional uncertainty in the rest of the circuit does not cause a problem.

The t_{PSK} specified optocouplers offer the advantages of guaranteed specifications for propagation delays, pulse-width distortion and propagation delay skew over the recommended temperature, input current, and power supply ranges.

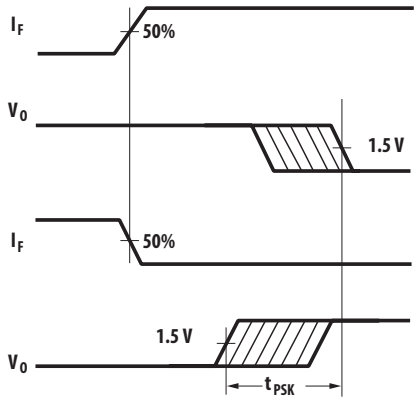


Figure 23. Propagation delay skew – t_{PSK}.

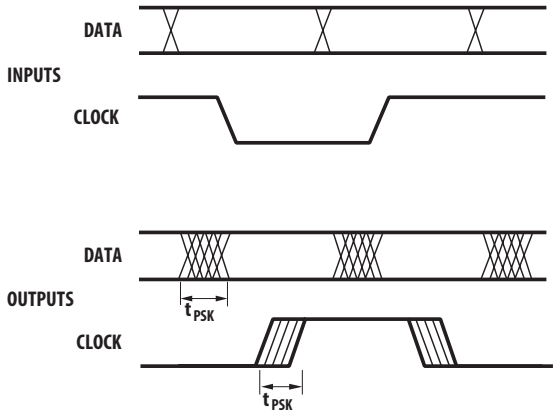


Figure 24. Parallel data transmission example.

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